What is claimed is:

1.   1.   A liquid crystal display apparatus comprising:
2.   a liquid crystal display panel comprising a matrix array of transistors
3.   and a matrix array of liquid crystal cells respectively connected to said
4.   transistors, said transistors being respectively connected to intersections of a
5.   plurality of column lines and a plurality of row lines for respectively
6.   activating the liquid crystal cells; and
7.   a driving circuit for successively generating a plurality of write-in
8.   voltages of a line signal of a video frame at end points of said column lines,
9.   successively selecting each of said row lines and supplying said write-in
10.   voltages from said end points of the column lines to the liquid crystal cells of
11.   the selected row line for a period corresponding to a geometric distance from
12.   the selected row line to said end points.

1.   2.   The liquid crystal display apparatus of claim 1, wherein said
2.   driving circuit comprises:
3.   a buffer memory for storing said video frame;
4.   a timing controller for generating first and second timing signals;
5.   a column driver for receiving a line signal from said memory,
6.   converting said line signal to said write-in voltages and supplying said write-
7.   in voltages to said column lines in response to said first timing signal; and
8.   a row driver for successively selecting each of said row lines for an
9.   interval between successive ones of said second timing signal and supplying
10.   said write-in voltages to the liquid crystal cells of the selected row line for a
11.   write-in period which runs from said first timing signal to said second timing
12.   signal,
13.   said timing controller generating said first timing signal at intervals
14.   increasingly variable as a function of the geometric distance from the selected
15.   row line to said column driver and generating said second timing signal at

16   said increasingly variable intervals.

1   3.   The liquid crystal display apparatus of claim 2, wherein said

2   write-in period is increasingly variable from a nominal value.

1   4.   The liquid crystal display apparatus of claim 2, wherein said

2   timing controller comprises:

3   a memory for storing a plurality of additive values, each of the

4   additive values corresponding to a geometric distance from the selected row

5   line to said column driver;

6   a line counter for incrementing a count number in response to a line

7   signal and reading an additive variable from said memory corresponding to

8   the count number;

9   an adder for summing the read variable with a constant value; and

10   variable-rate pulse generating means for producing each of said first

11   and second timing signals at intervals corresponding to an output signal of

12   said adder.

1   5.   The liquid crystal display apparatus of claim 1, wherein said

2   driving circuit comprises:

3   a timing controller for generating a first, second and third timing

4   signals;

5   a column driver for converting a line signal to said write-in voltages

6   and supplying said write-in voltages to said column lines in response to the

7   first timing signal;

8   a row driver for successively selecting one of said row lines for an

9   interval between successive ones of said second timing signal and supplying

10   said write-in voltages to the liquid crystal cells of the selected row line for a

11   write-in period which runs from said first timing signal to said third timing

12   signal,

13   said timing controller generating each of said first and second timing

14   signals at constant intervals and generating said third timing signal at

15   intervals increasingly variable as a function of the geometric distance from

16   the selected row line to said column driver.

1   6.   The liquid crystal display apparatus of claim 5, wherein said

2   write-in period is variable from a less-than-nominal value to a nominal value.

1   7.   The liquid crystal display apparatus of claim 5, wherein said

2   timing controller comprises:

3   a memory for storing a plurality of subtractive values, each of the

4   subtractive values corresponding to a geometric distance from the selected

5   row line to said column driver;

6   a line counter for incrementing a count number in response to a line

7   signal and reading a subtractive value from said memory corresponding to

8   the count number;

9   a subtractor for subtracting the read subtractive value from a constant

10   value;

11   constant-rate pulse generating means for producing each of said first

12   and second timing signals at constant intervals; and

13   variable-rate pulse generating means for producing said third timing

14   signal at intervals corresponding to an output signal of said subtractor.

1   8.   The liquid crystal display apparatus of claim 1, wherein said

2   driving circuit comprises:

3   a buffer memory for storing said video frame;

4   a timing controller for generating first, second, third, fourth and fifth

5   timing pulses;

6   a column driver for receiving a line signal from said memory,

7   converting said line signal to said write-in voltages and supplying said write-

8   in voltages to said column lines in response to said first timing signal during

9   a first portion of a frame interval and in response to said fourth timing signal

10   during a second portion of the frame interval;

11   a row driver for successively selecting one of said row lines for an

12   interval between successive ones of said second timing signal during said

13   first portion of the frame interval and supplying said write-in voltages to the

14   liquid crystal cells of the selected row line for a write-in period which runs

15   from said first timing signal to said third timing signal, successively selecting

16   one of said row lines for an interval between successive ones of said fifth

17   timing signal during said second portion of the frame interval and interval,

18   and supplying said write-in voltages to the liquid crystal cells of the selected

19   row line for a write-in period which runs from said fourth timing signal to

20   said fifth timing signal,

21   said timing generator generating, during said first portion of the frame

22   interval, each of said first and second timing signals at constant intervals and

23   said third timing signal at intervals increasingly variable as a function of the

24   geometric distance from the selected row line to said column driver and

25   generating, during said second portion of the frame interval, each of said

26   fourth and fifth timing signals at intervals increasingly variable as a function

27   of the geometric distance from the selected row line to said column driver.

1   9.   The liquid crystal display apparatus of claim 8, wherein said

2   write-in period of said first portion of the frame interval is increasingly

3   variable from a less-than-nominal value to a nominal value and the said

4   write-in period of said second portion of the frame interval is increasingly

5   variable from said nominal value.

1   10.   The liquid crystal display apparatus of claim 8, wherein said

2   timing controller comprises:

3   a memory for storing a plurality of subtractive values and a plurality

4   of additive values, each of said subtractive and additive values

5   corresponding to a geometric distance from the selected row line to said

6   column driver;

7   a line counter for incrementing a count number in response to a line

8   signal and reading one of said subtractive values from said memory

9   corresponding to the count number during said first portion of the frame

10   interval and reading one of said additive values from said memory

11   corresponding to the count number during said second portion of the frame

12   interval;

13   a subtractor for subtracting from a constant value the subtractive value

14   which is read from said memory during said first portion of the frame

15   interval;

16   an adder for summing said constant value with the additive value

17   which is read from said memory during said second portion of the frame

18   interval;

19   constant-rate pulse generating means for producing each of said first

20   and second timing signals at constant intervals; and

21   variable-rate pulse generating means for producing said third timing

22   signal at intervals corresponding to an output signal of said subtractor and

23   producing each of said fourth and fifth timing signal at intervals

24   corresponding to an output signal of said adder.

1   11.   A method of driving a liquid crystal display, wherein the liquid

2   crystal display panel comprises a matrix array of transistors and a matrix

3   array of liquid crystal cells respectively connected to said transistors, said

4   transistors being respectively connected to intersections of a plurality of

5   column lines and a plurality of row lines for respectively activating the liquid

6   crystal cells, the method comprising the steps of:

7   a)   generating a plurality of write-in voltages of a line signal of a

8   video frame so that the write-in voltages appear at end points of said column

9   lines;

10   b)   successively selecting one of said row lines; and

11   c)   successively supplying said write-in voltages from said end

12   points of the column lines to the liquid crystal cells of the selected row line

13   for a write-in period corresponding to the geometric distance from the

14   selected row line to said end points.

1   12.   The method of claim 11, wherein step (a) comprises the step of

2   buffering said line signal in a memory and wherein step (c) comprises the

3   step of increasingly varying said write-in period from a nominal value as a

4   function of said geometric distance.

1   13.   The method of claim 11, wherein step (c) comprises the step of

2   increasingly varying said write-in period as a function of said geometric

3   distance in a range from a less-than-nominal value to a nominal value.

1   14.   The method of claim 11, wherein step (a) comprises the step of

2   buffering said line signal in a memory and wherein step (d) comprises the

3   step of increasingly varying said write-in period as a function of said

4   geometric distance in a range from a less-than-nominal value to a nominal

5   value during a first portion of a frame interval and increasingly varying said

6   write-in period as a function of said geometric distance from the nominal

7   value.

1   15.   A driving circuit for a liquid crystal display which comprises a

2   matrix array of transistors and a matrix array of liquid crystal cells

3   respectively connected to said transistors, said transistors being respectively

4   connected to intersections of a plurality of column lines and a plurality of row

5   lines for respectively activating the liquid crystal cells, the driving circuit

6   comprising means for successively generating a plurality of write-in voltages

7   of a line signal of a video frame at end points of said column lines,

8   successively selecting each of said row lines and supplying said write-in

9   voltages from said end points of the column lines to the liquid crystal cells of

10   the selected row line for a period corresponding to a geometric distance from

11   the selected row line to said end points.

1   16.   The driving circuit of claim 15, wherein said means comprises:

2   a buffer memory for storing said video frame;

3   a timing controller for generating first and second timing signals;

4   a column driver for receiving a line signal from said memory,

5   converting said line signal to said write-in voltages and supplying said write-

6   in voltages to said column lines in response to said first timing signal; and

7   a row driver for successively selecting each of said row lines for an

8   interval between successive ones of said second timing signal and supplying

9   said write-in voltages to the liquid crystal cells of the selected row line for a

10   write-in period which runs from said first timing signal to said second timing

11   signal,

12   said timing controller generating said first timing signal at intervals

13   increasingly variable as a function of the geometric distance from the selected

14   row line to said column driver and generating said second timing signal at

15   said increasingly variable intervals.

1   17.   The driving circuit of claim 16, wherein said write-in period is

2   increasingly variable from a nominal value.

1   18.   The driving circuit of claim 16, wherein said timing controller

2   comprises:

3   a memory for storing a plurality of additive values, each of the

4   additive values corresponding to a geometric distance from the selected row

5   line to said column driver;

6   a line counter for incrementing a count number in response to a line

7   signal and reading an additive variable from said memory corresponding to

8   the count number;

9   an adder for summing the read variable with a constant value; and

10   variable-rate pulse generating means for producing each of said first

11 and second timing signals at intervals corresponding to an output signal of

12 said adder.

1   19.   The driving circuit of claim 15, wherein said driving circuit

2   comprises:

3   a timing controller for generating a first, second and third timing

4   signals;

5   a column driver for converting a line signal to said write-in voltages

6   and supplying said write-in voltages to said column lines in response to the

7   first timing signal;

8   a row driver for successively selecting one of said row lines for an

9   interval between successive ones of said second timing signal and supplying

10 said write-in voltages to the liquid crystal cells of the selected row line for a

11 write-in period which runs from said first timing signal to said third timing

12 signal,

13   said timing controller generating each of said first and second timing

14 signals at constant intervals and generating said third timing signal at

15 intervals increasingly variable as a function of the geometric distance from

16 the selected row line to said column driver.

1   20.   The driving circuit of claim 19, wherein said write-in period is

2   variable from a less-than-nominal value to a nominal value.

1   21.   The driving circuit of claim 19, wherein said timing controller

2   comprises:

3   a memory for storing a plurality of subtractive values, each of the

4 subtractive values corresponding to a geometric distance from the selected

5 row line to said column driver;

6   a line counter for incrementing a count number in response to a line

7 signal and reading a subtractive value from said memory corresponding to

8 the count number;

9   a subtractor for subtracting the read subtractive value from a constant

10 value;

11   constant-rate pulse generating means for producing each of said first

12 and second timing signals at constant intervals; and

13   variable-rate pulse generating means for producing said third timing

14 signal (VOE) at intervals corresponding to an output signal of said subtractor.

1   22. The driving circuit of claim 15, wherein said means comprises:

2   a buffer memory for storing said video frame;

3   a timing controller for generating first, second, third, fourth and fifth

4 timing pulses;

5   a column driver for receiving a line signal from said memory,

6 converting said line signal to said write-in voltages and supplying said write-

7 in voltages to said column lines in response to said first timing signal during

8 a first portion of a frame interval and in response to said fourth timing signal

9 during a second portion of the frame interval;

10   a row driver for successively selecting one of said row lines for an

11 interval between successive ones of said second timing signal during said

12 first portion of the frame interval and supplying said write-in voltages to the

13 liquid crystal cells of the selected row line for a write-in period which runs

14 from said first timing signal to said third timing signal, successively selecting

15 one of said row lines for an interval between successive ones of said fifth

16 timing signal during said second portion of the frame interval and interval,

17 and supplying said write-in voltages to the liquid crystal cells of the selected

18 row line for a write-in period which runs from said fourth timing signal to

19 said fifth timing signal,

20   said timing generator generating, during said first portion of the frame

21 interval, each of said first and second timing signals at constant intervals and

22 said third timing signal at intervals increasingly variable as a function of the

23 geometric distance from the selected row line to said column driver and

24 generating, during said second portion of the frame interval, each of said

25 fourth and fifth timing signals at intervals increasingly variable as a function

26 of the geometric distance from the selected row line to said column driver.

1   23.   The driving circuit of claim 22, wherein said write-in period of

2 said first portion of the frame interval is increasingly variable from a less-

3 than-nominal value to a nominal value and the said write-in period of said

4 second portion of the frame interval is increasingly variable from said

5 nominal value.

1   24.   The driving circuit of claim 22, wherein said timing controller

2 comprises:

3   a memory for storing a plurality of subtractive values and a plurality

4 of additive values, each of said subtractive and additive values

5 corresponding to a geometric distance from the selected row line to said

6 column driver;

7   a line counter for incrementing a count number in response to a line

8 signal and reading one of said subtractive values from said memory

9 corresponding to the count number during said first portion of the frame

10 interval and reading one of said additive values from said memory

11 corresponding to the count number during said second portion of the frame

12 interval;

13   a subtractor for subtracting from a constant value the subtractive value

14 which is read from said memory during said first portion of the frame

15 interval;

16 an adder for summing said constant value with the additive value

17 which is read from said memory during said second portion of the frame

18 interval;

19 constant-rate pulse generating means for producing each of said first

20 and second timing signals at constant intervals; and

21 variable-rate pulse generating means for producing said third timing

22 signal at intervals corresponding to an output signal of said subtractor and

23 producing each of said fourth and fifth timing signals at intervals

24 corresponding to an output signal of said adder.